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Sheet 1 of 2

Complete if Known	
Application Number	10/724,876
Filing Date	December 2, 2003
First Named Inventor	Haitham H. AKKARY et al.
Group Art Unit	2181
Examiner Name	Not Yet Assigned
Attorney Docket Number	42339-193264

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AL	A1	6,591,342	B1	AKKARY et al.	07-08-2003	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
AL	A2	BALASUBRAMONIAN et al., "Reducing the Complexity of the Register File in Dynamic Superscalar Processors", In *Proceedings of the 34th International Symposium on Microarchitecture*, Dec. 2001, pgs. 237-248.	
AL	A3	BREKELBAUM et al., "Hierarchical Scheduling Windows", In *Proceedings of the 35th International Symposium on Microarchitecture*, Nov. 2002, pgs. 27-36.	
AL	A4	BROWN et al., "Select-Free Instruction Scheduling Logic", In *Proceedings of the 34th International Symposium on Microarchitecture*, Dec. 2001, pgs. 204-213.	
AL	A5	ZALAMEA et al., "Two-level Hierarchical Register File Organization for VLIW Processors", In *Proceedings of the 33rd International Symposium on Microarchitecture*, Dec. 2000, pgs. 137-146.	
AL	A6	CANAL et al., "A Low-Complexity Issue Logic", In *Proceedings of the 2000 International Conference on Supercomputing*, Jun. 2000, pgs. 327-335.	
AL	A7	CAPITANIO et al., "Partitioned Register Files for VLIWs: A Preliminary Analysis of Tradeoffs", In *Proceedings of the 25th Int'l Symposium on Microarchitecture*, Dec. 1992, pgs. 292-300.	
AL	A8	GOPAL et al., "Speculative Versioning Cache", In *Proceedings of the Fourth International Symposium on High-Performance Computer Architecture*, Feb. 1998, pgs 195-205.	
AL	A9	HAMMOND et al., "Data Speculation Support for a Chip Multiprocessor", In *Proceedings of the Eighth Symposium on Architectural Support for Programming Languages and Operating Systems*, Oct. 1998, pgs. 58-69.	
AL	A10	HENRY et al., "Circuits for Wide-Window Superscalar Processors", In *Proceedings of the 27th Annual International Symposium on Computer Architecture*, June 2000, pgs. 236-247.	
AL	A11	HINTON et al., "The Microarchitecture of the Pentium ® 4 Processor", *Intel Technology Journal* Q1, Feb. 2001, pgs. 1-13.	
AL	A12	JACOBSEN et al., "Assigning Confidence to Conditional Branch Predictions", In *Proceedings of the 29th International Symposium on Microarchitecture*, Dec. 1996, pgs. 142-152.	
AL	A13	KARKHANIS et al., "A Day in the Life of a Data Cache Miss", In *Workshop on Memory Performance Issues*, 2002, pgs. 1-10.	
AL	A14	KNIGHT, "An Architecture for Mostly Functional Languages", In *Proceedings of ACM Lisp and Functional Programming Conference*, Aug. 1986, pgs. 500-519 (reprint pgs. 105-112).	

AL	A15	LEBECK et al., "A Large, Fast Instruction Window for Tolerating Cache Misses", In *Proceedings of the 29th Annual International Symposium on Computer Architecture*, May 2002, pgs. 59-70.	
AL	A16	LEIBHOLZ et al., "The Alpha 21264: A 500 MHz Out-of-Order Execution Microprocessor", In *Proceedings of the 42nd IEEE Computer Society International Conference* (COMPCON), Feb. 1997, pgs. 28-36.	
AL	A17	MARTINEZ et al., "Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors", In *Proceedings of the 35th International Symposium on Microarchitecture*, Nov. 2002, pgs. 3-14.	
AL	A18	MICHAUD et al., "Data-Flow Prescheduling for Large Instruction Windows in Out-of-Order Processors", In *Proceedings of the Seventh International Symposium on High-Performance Computer Architecture*, Jan. 2001, pgs. 27-36.	
AL	A19	MOUDGILL et al., "Register Renaming and Dynamic Speculation: An Alternative Approach", In *Proceedings of the 26th International Symposium on Microarchitecture*, Dec. 1993, pgs. 202-213.	
AL	A20	PALACHARLA et al., "Complexity-Effective Superscalar Processors", In *Proceedings of the 24th Annual International Symposium on Computer Architecture*, June 1997, pgs. 206-218.	
AL	A21	RANGANATHAN et al., "Using Speculative Retirement and Larger Instruction Windows to Narrow the Performance Gap between Memory Consistency Models", In *Proceedings on the 9th Annual ACM Symposium on Parallel Algorithms and Architectures*, Jun. 1997, pgs. 199-210.	
AL	A22	ROTENBERG et al., "Trace Processors",In *Proceedings of the 30th International Symposium on Microarchitecture*, June 1997, pgs. 138-148.	
AL	A23	SMITH et al., "Implementation of Precise Interrupts in Pipelined Processors", In *Proceedings of the 12th Annual International Symposium on Computer Architecture*, June 1985, pgs. 36-44.	
AL	A24	SPRANGLE et al., "Increasing Processor Performance by Implementing Deeper Pipelines", In *Proceedings of the 29th Annual International Symposium on Computer Architecture*, May 2002, pgs. 25-34.	
AL	A25	STEFFAN et al., "A Scalable Approach to Thread-Level Speculation", In *Proceedings of the 27th Annual International Symposium on Computer Architecture*, June 2000, pgs. 1-12.	
AL	A26	TENDLER et al., "POWER4 System Microarchitecture", IBM J. Res. & Dev., vol. 46, no. 1, January 2002, pgs. 5-25,	
AL	A27	VIJAYAN et al., "Out-of-Order Commit Logic With Precise Exception Handling For Pipelined Processors", In *Poster in High Performance Computer Conference*, Dec. 2002.	
AL	A28	HWU et al., "Checkpoint Repair for Out-of-order Execution Machines", In *Proceedings of the 14th Annual International symposium on Computer architecture*, 1987, pgs. 18-26.	
AL	A29	YEAGER, "The MIPS R10000 Superscalar Microprocessor", IEEE Micro, April 1996, pgs. 28-40.	

Examiner Signature	/Aimee Li/	Date Considered	10/05/2006

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